

JUN 04 2004
JULY 9 2004
TRADEMARK OFFICE

FIELD OF THE INVENTION

BACKGROUND OF THE INVENTION

An important area in modern electronics is so-called polymer electronics, in which polymer materials are used as a material for forming electrical circuits or circuit components.—[2] C.D. Dimitrakopoulos, D.J. Masearo (2001) "Organic thin film transistors". IBM J. Res.&Dev. 45, pp. 11-27. provides an overview of organic thin film transistors based on polymer materials.

Problems arise if a reference voltage source is intended to be formed in the context of polymer electronics, since to date there is no satisfactory technical solution for diodes in the context of a simple polymer technology.

The polymer transistor arrangement according to the invention has a polymer transistor formed in and/or on a substrate. The polymer transistor contains a first source/drain region, a second source/drain region, a channel region between the first and second source/drain regions and also a gate region. The polymer transistor furthermore contains a gate-insulating layer between channel region and gate region. The polymer transistor arrangement furthermore has a drive circuit which is set up in such a way that it provides the source/drain regions and the gate region with electrical potentials such that the junction between at least one of the source/drain regions and the channel region can be operated as a diode.

Furthermore, the invention provides an integrated circuit arrangement having at least one polymer transistor arrangement having the features described.

In accordance with the invention's method for producing a polymer transistor arrangement, a polymer transistor is formed in and/or on a substrate by a first source/drain region being formed, a second source/drain region being formed and a channel region being formed between the first and second source/drain regions. Furthermore, a gate region is formed. A gate-insulating layer is furthermore formed between channel region and gate region. Furthermore, a drive circuit of the polymer transistor arrangement according to the invention is formed and set up in such a way that it provides the source/drain regions and the gate region with electrical potentials such that the junction between at least one of the source/drain regions and the channel region is operated as a diode.

A fundamental idea of the invention is based on connecting up a junction between one of the source/drain regions of a polymer transistor and the channel region in such a way that it can be used as a diode. A suitable operating point is chosen for this by applying to

According to the invention, a polymer transistor is clearly connected up in such a way that the junction between one of the source/drain regions and the channel region is set up or can be operated as a diode. The polymer transistor is clearly connected up in such a way that it represents a gate-controlled diode.

It should be noted that both the polymer transistor and the drive circuit may be formed completely in polymer technology.

Preferred developments of the invention emerge from the dependent claims.

The drive circuit may be set up in such a way that it applies electrical potentials to the source/drain regions and to the gate region such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-biased diode. In this case, the junction between the other of the two source/drain regions and the channel region is connected as a forward-biased diode. The reverse-biased diode is then dominant for the non-reactive resistance of the polymer transistor arrangement.

The value of the electrical potentials applied to the source/drain regions for the purpose of controlling the diode may be chosen on the basis of the thickness and/or the value of the dielectric constant of the gate-insulating layer of the polymer transistor. The value of the gate voltage may also be set on the basis of these or other criteria. Preferably, the value (in terms of magnitude) of the gate voltage is chosen to be essentially proportional to the value of the dielectric constant of the gate-insulating layer.

A metallic or a polymer material may be used as material of the source/drain regions of the polymer transistor arrangement. A polymer material is preferably used for the channel region. When using a first polymer material for the source/drain regions and a second polymer material for the channel region, the junction between the first and second

For this purpose, one of the source/drain regions may be formed at least partially on the organic semiconductor and the other source/drain region may be formed at least partially below the organic semiconductor. In this case, a significantly better conductivity results with the contact arranged above the organic semiconductor, so that the diode junction at the other contact dominates the current flow.

The integrated circuit arrangement according to the invention, which has at least one polymer transistor arrangement according to the invention, is described in more detail below. Refinements of the integrated circuit arrangement also apply to the polymer transistor arrangement, and vice-versa.

The integrated circuit arrangement may be set up as a reference voltage circuit, preferably as a temperature-compensated reference voltage circuit.


The integrated circuit arrangement may also be set up as a current source.

Furthermore, the integrated circuit arrangement may be set up as a voltage control circuit.

The integrated circuit arrangement may also be set up as a combination of the circuit types mentioned. For example, the integrated circuit arrangement according to the invention may have a current source with a first polymer transistor arrangement and a reference voltage source with a second polymer transistor arrangement.

Furthermore, apart from the polymer transistor or transistors, other components of the integrated circuit according to the invention may also be produced from polymer material. By way of example, an operational amplifier may likewise be formed in polymer electronics.

BRIEF DESCRIPTION OF THE DRAWINGS

{W:\20046\0200501us0\00128084.DOC  }

DETAILED DESCRIPTION OF THE PREFERRED MODE OF THE INVENTION

Identical or similar components in different figures are provided with the same reference numerals.

A polymer transistor arrangement 100 in accordance with one exemplary embodiment of the invention is described below with reference to figure 1.

The polymer transistor arrangement 100 has a polymer transistor formed on a substrate 101. Said polymer transistor contains a gate region 106 made of titanium material, which is formed on the substrate 101. A PVP layer (polyvinylphenol) is formed as gate-insulating layer 105 on the gate region 106. The gate-insulating layer 105 is formed by means of the application of PVP material and by means of the photolithographic patterning of the layer of PVP material, as a result of which the gate-insulating layer 105 remains. A first source/drain region 102 made of gold material is formed on one part of the substrate 101 and on one part of the gate-insulating layer 105. A second source/drain region 103 made of gold material is formed on another part of the substrate 101 and on another part of the gate-insulating layer 105. Furthermore, an active pentacene layer is formed on both source/drain regions 102, 103 and on a region of the gate-insulating layer 105 that is arranged between said source/drain regions, the central section of which pentacene layer serves as channel region 104. It should be noted that pentacene is an organic semiconducting material. At least some of the components of the polymer transistor may be printed on. By means of a drive circuit 107, which is electrically coupled to the two source/drain regions 102, 103 and to the gate region 106 by means of electrically conductive coupling means 108, the source/drain regions 102, 103 and the gate region 105 are in each

case provided with an electrical potential such that the junction between one of the source/drain regions 102 or 103 and the channel region 104 can be operated as a diode.

The gate-insulating layer 105 may alternatively be produced from silicon oxide (e.g., generated by means of thermal oxidation of silicon material), aluminum oxide or PVP (polyvinylphenol). The gate region 106 may alternatively also be produced from palladium or gold. Examples of polymer materials which can be used for forming the polymer transistor according to the invention or other circuit components are primarily recurring chains of carbon-containing molecules. For example, it is possible to use pentacene, poly(3-hexylthiophene), organic-inorganic hybrids such as $(C_6H_5C_2H_4NH_3)_2SnI_4$, C_{60} or α,ω -dihexylquinquethiophene (DH α 5T).

An equivalent circuit diagram 200 of the polymer transistor connected up according to the invention is described below with reference to figure 2.

The equivalent circuit diagram 200 shows the components from figure 1 and also a first diode 201 as a circuitry equivalent of the junction between the first source/drain region 102 and the channel region 104 and also a second diode 202 as a circuitry equivalent of the junction between the channel region 104 and the second source/drain region 103. The diagram further depicts first and second non-reactive resistors 203, 204 for modeling contact effects in figure 2, which are arranged between a respective one of the source/drain regions 102, 103, on the one hand, and a respective terminal of a respective diode 201, 202, on the other hand.

It is clearly the case that, according to the invention, the operating point of the polymer transistor arrangement 100 is set by application of suitable electrical voltages, which are applied to the terminals 102, 103, 106 by means of the drive circuit 107 in such a

way that only one of the two diodes 201, 202 shown in figure 2 functions as a diode in circuitry terms, whereas the other of the two diodes has a very low impedance. As an alternative, it is also possible for both diodes 201, 202 to be operated as diodes. Figure 2 diagrammatically indicates that the diodes 201, 202 are also influenced by means of an electrical potential applied to the gate region 106.

If the voltage drop across the diode 201 is designated as V_{d1} , the voltage drop across the diode 202 is designated as V_{d2} , the voltage drop across the channel region 104 is designated as V_i , the voltage between the first source/drain region 102 and the gate region 106 is designated as V_{gs} , the voltage between the second source/drain region 103 and the gate region 106 is designated as V_{gd} , and the voltage between the source/drain regions 102, 103 is designated as V_{ds} , then the voltages should fulfill the following relationships in terms of magnitude:

$$V_{gs} > V_{gd} \gg V_{ds}; V_{d1} > V_{d2} \gg V_i$$

In this case, primarily the first diode 201 functions as a diode also in circuitry terms.

A description is given below, with reference to the diagram 300 from figure 3, of how the operating point of the polymer transistor arrangement 100 is chosen in order to operate one of the two junctions between one of the two source/drain regions 102, 103, on the one hand, and the channel region 104, on the other hand, as a diode.

In the diagram 300, the electrical voltage between the two source/drain regions 102, 103 is plotted along an abscissa 301. The electric current at the second source/drain terminal 103 is plotted along an ordinate 302. Furthermore, figure 3 shows first to third characteristic curves 303 to 305, the first characteristic curve 303 corresponding to a voltage between the gate region 105 and the first source/drain region 102 of 0 volts, the second

characteristic curve 304 corresponding to a voltage of -5 volts and the third characteristic curve 305 corresponding to a voltage of -10 volts.

In the example shown in figure 3, the operating points which correspond to the third characteristic curve 305 are well suited to operating the polymer transistor arrangement 100 in such a way that one of the two diodes 201, 202 can actually be operated as a diode. What is particularly well suited is the operating range on the third characteristic curve 305 in the region of voltages of small magnitude between the two source/drain regions 102, 103, i.e., in the top right region of the diagram 300 in accordance with figure 3.

At a suitable operating point, the voltage (in terms of magnitude) between the gate region 106 and the first source/drain region 102 is given by the oxide capacitance per area (the magnitude of the voltage between the gate region 106 and the first source/drain region 102 is approximately indirectly proportional thereto). Furthermore, the electrical voltage between the gate region 106 and the first source/drain region 102 should be as large as possible in terms of magnitude, that is to say as near as possible to a maximum permissible voltage. By contrast, the magnitude of the voltage between the two source/drain regions 102, 103 should be as near as possible to 0 volts. The maximum permissible voltage primarily depends on the quality (in particular on the output transconductance) of the polymer transistor. If the value of the output transconductance is small relative to the diode conductance of the Schottky junction, then the Schottky diode dominates the electric current and the transistor behaves like a diode at this operating point.

A description is given below, with reference to figure 4, of a reference voltage circuit 400 as an integrated circuit arrangement in accordance with a first exemplary embodiment of the invention.

{W:\20046\0200501us0\00128084.DOC [REDACTED] }

In the case of the reference voltage circuit 400, an input voltage 401 V_{in} is applied between the electrical ground potential 402 and a first terminal of a current source 403. A reference voltage 404 V_{ref} is present between the other terminal of the current source 403 and the electrical ground potential 402. Furthermore, the first source/drain region 102 of a polymer transistor 406 is coupled to the second terminal of the current source 403. The second source/drain region 103 of the polymer transistor 403 is at the electrical ground potential 402. The bias voltage 405 V_{bias} is applied to the gate region 106.

The polymer transistor 406, by application of the bias voltage V_{bias} , is brought to an operating point such that it operates like a Schottky diode. In accordance with the predetermined operating point, a gate voltage of large magnitude and drain voltages of small magnitude are applied to the terminals of the polymer transistor 406. In the path between the input voltage 401 V_{in} and the reference voltage 404 V_{ref} , a constant electric current flows through the current source 403. If an increased electric current is tapped off at the node of the reference voltage 404 V_{ref} , at the same time a smaller electric current flows through the polymer transistor 406, since otherwise the electrical voltage at the reference voltage 404 V_{ref} is greatly reduced and, consequently, exponentially less current can flow through the polymer transistor 406. The setting of the bias voltage 405 V_{bias} is not all that sensitive with regard to the size of the electric current as long as one is in the suitable operating point range. Therefore, in many cases the input voltage 401 V_{in} may be provided jointly with the bias voltage 405.

It is clearly the case in the reference voltage circuit 400 shown in figure 4 that the diode between the channel region 104 and the second source/drain region 103 is connected as zener diode for voltage stabilization purposes. The unstabilized input voltage V_{in} 401 is

{W:\20046\0200501us0\00128084.DOC [REDACTED] }

A description is given below, with reference to figure 6, of a voltage control circuit 600 as an integrated circuit arrangement in accordance with a third exemplary embodiment of the invention.

The voltage control circuit 600 has an operational amplifier 602 provided with an operating voltage 601. Furthermore, the operational amplifier 602 is provided with the ground potential 402 as lower voltage reference point. An output 602c of the operational amplifier 602 is fed back to a non-inverting input 602a of the operational amplifier 602 via a first non-reactive resistor 603. Furthermore, the output 602c is fed back to an inverting input 602b of the operational amplifier 602 via a second non-reactive resistor 604. Moreover, the output 602c is at the reference voltage 404 V_{ref} . A third non-reactive resistor 605 is connected between the second non-reactive resistor 604 and the electrical ground potential 402. The two source/drain terminals 102, 103 of the polymer transistor 406 are connected between the first non-reactive resistor 603 and the electrical ground potential 402. The bias voltage 405 V_{bias} is applied to the gate terminal 106 of the polymer transistor 406.

The stabilized reference voltage V_{ref} 404 is determined by means of the second and third non-reactive resistors 604, 605. The electric current through the polymer transistor 406 has the effect of holding the voltage V_{ref} at a constant value, which is clearly defined by means of the kink voltage of the Schottky diode of the polymer transistor 406. Fluctuations in the operating voltage 601 V_{dd} are suppressed by the common-mode rejection of the operational amplifier 602.

The polymer transistor 406 in the voltage control circuit 600 again serves as a replacement for a zener diode. That Schottky diode of the polymer transistor 406 which is

connected between the fourth non-reactive resistor 706 and the electrical ground potential 402. The fourth non-reactive resistor 706 is coupled to a first source/drain region of another polymer transistor 501. The second source/drain region of the other polymer transistor 501 is coupled to the second non-reactive resistor 704 and to the inverting input 702b of the operational amplifier 702. The gate terminal of the other polymer transistor 501 is coupled to the gate terminal of the polymer transistor 406. Furthermore, a sixth non-reactive resistor 708 is connected between the gate region of the other polymer transistor 501 and the electrical ground potential 402.

Using the property of the operational amplifier 702 of subtracting from one another the electrical voltages provided at two inputs 702a, 702b, it is possible to generate the voltage reference circuit 700, which compensates in particular linear temperature gradients of the components of the circuit. In the case of the temperature-compensated reference voltage circuit 700, the first and second non-reactive resistors 703, 704 are dimensioned in such a way that the same electrical voltage is dropped across them. By means of the fourth non-reactive resistor 706, a small voltage difference is generated between the source/drain terminals of the polymer transistors 406, 501. The change in the electric current at the fifth non-reactive resistor 707 in the event of a change in temperature then depends on the dimensioning of the two transistors 406, 501 relative to one another (for example the dimensioning of the gate widths of said transistors). Since the electric currents through the two transistors 406, 501 lead to a voltage drop across the fifth non-reactive resistor 707, the temperature-dependent change thereof also leads to a corresponding voltage drop across the fifth non-reactive resistor 707. If the characteristics of the two transistors 406, 501 and of the fifth non-reactive resistor 707 are set in such a way that the change in voltage in the

event of a change in the temperature is compensated for sufficiently exactly by the change in the influence of the gate voltage on the polymer transistors 406, 501, then the circuit 700 is free of a (linear) temperature response and constitutes a temperature-compensated voltage source. The gate voltage at the polymer transistors 406, 501 is furthermore to be set in such a way that the two polymer transistors 406, 501 have a sufficiently large voltage difference in terms of magnitude between the respective gate terminal and one of the two source/drain terminals and the current through the polymer transistors 501, 406 leads to only a small voltage drop.

A description is given below, with reference to figure 8, of a polymer transistor 800 of a polymer transistor arrangement according to the invention in accordance with a preferred exemplary embodiment of the invention.

The polymer transistor 800 has a substrate 101 with a first and a second surface region, a metallic gate region 106 being applied on the first surface region. A first source/drain region 102 made of gold material is applied on the second surface region. A gate-insulating layer 105 is formed on the gate region. Furthermore, a channel region 104 made of a semiconducting polymer is formed on a surface region of the layer sequence thus obtained, which channel region 104 covers both the gate region 106 covered with the gate-insulating layer 105 and the first source/drain region 102. A second source/drain region 103 made of gold material is formed partially on the substrate 101 and partially on the channel region 104.

As shown in figure 8, the junction regions between a respective one of the source/drain regions 102, 103, on the one hand, and the channel region 104, on the other hand, are formed geometrically asymmetrically with respect to one another. The second

source/drain region 103 is formed partially on the channel region 104, and the first source/drain region 102 is essentially formed below the channel region 104. This asymmetrical arrangement of the two source/drain regions with respect to one another means that the junction regions between a respective one of the source/drain regions 102, 103 and the respectively adjoining part of the channel region 104, at least one of which junctions is operated as a diode according to the invention, have different structural properties. These structural properties lead to different functional-physical properties of the two junction regions. It is clearly the case when the two junctions are provided asymmetrically that it is possible technologically to support the situation in which the different junctions can be operated in a different functionality by application of different electrical potentials to the terminals of the polymer transistor. Thus, according to the invention, by way of example, one of the junctions may be embodied at sufficiently low impedance such that it hardly influences the current flow, and the other junction may be connected up as a conductive diode. This can be supported geometrically.

A description is given below, with reference to figure 9, of a polymer transistor 900 of a polymer transistor arrangement according to the invention in accordance with another preferred exemplary embodiment of the invention.

A gate region 106 is formed on a substrate 101, which gate region is covered with a gate-insulating layer 105. A first source/drain region 102 is formed in a manner partially adjoining the gate-insulating layer 105 and partially on the substrate 101. The components formed are covered with semiconducting polymer material as channel region 104. A second source/drain region 103 is formed partially on the substrate 101 and partially on the channel region 104.

The polymer transistor arrangement 900 also has a pronounced geometrical asymmetry with regard to the two source/drain regions 102, 103. This again brings about a significant difference in the physical properties of the junctions between one of the source/drain regions 102, 103 and the channel region 104. As a result, it is possible to structurally support the invention's driving of these junctions as blocking or as conductive diodes.

~~The following publications are cited in this document:~~

- ~~{1} U. Tietze, C. Schenk "Halbleiterschaltungstechnik"
["Semiconductor circuitry"], Springer Verlag, Berlin,
1993, pp. 555-560~~
- ~~{2} C.D. Dimitrakopoulos, D.J. Masearo (2001) "Organic thin
film transistors", IBM J. Res.&Dev. 45, pp. 11-27~~
- ~~{3} P.V. Neeliudov, M.S. Shur, D.J. Gundlach, T.N. Jackson
(2000) "Modeling of organic thin film transistors of
different designs" J.Appl.Phys. 88, pp. 6594-6597~~
- ~~{4} WO 01/01452 A2~~
- ~~{5} US 6,455,873 B1~~
- ~~{6} Nährmann, D "Das große Werkbuch Elektronik" ["The large
workbook of electronics"], Volume 2, 1998, Franzis-
Verlag Poing, ISBN 3-7723-6547-7, pages 1415-1423~~

List of reference symbols

100	Polymer transistor arrangement
101	Substrate
102	First source/drain region
103	Second source/drain region
104	Channel region
105	Gate insulating layer
106	Gate region
107	Drive circuit
108	Coupling means
200	Equivalent circuit diagram
201	First diode
202	Second diode
203	First non-reactive resistor
204	Second non-reactive resistor
300	Diagram
301	Abseissa
302	Ordinate
303	First characteristic curve
304	Second characteristic curve
305	Third characteristic curve
400	Reference voltage circuit
401	Input voltage
402	Ground potential
403	Current source
404	Reference voltage
405	Bias voltage
406	Polymer transistor
500	Reference voltage circuit
501	Other polymer transistor
502	Other bias voltage
600	Voltage control circuit
601	Operating voltage
602	Operational amplifier

{W:\20046\0200501us0\00128084.DOC [REDACTED] }

602a	Non-inverting input
602b	Inverting input
602e	Output
603	First non-reactive resistor
604	Second non-reactive resistor
605	Third non-reactive resistor
700	Temperature-compensated reference voltage circuit
701	Supply voltage
702	Operational amplifier
702a	Non-inverting input
702b	Inverting input
702e	Output
703	First non-reactive resistor
704	Second non-reactive resistor
705	Third non-reactive resistor
706	Fourth non-reactive resistor
707	Fifth non-reactive resistor
708	Sixth non-reactive resistor
800	Polymer transistor
900	Polymer transistor